REMARKS

Claims 1, 7, 16, and 21 have been amended. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 13 and 27 have been cancelled. No claims have been added. Hence, claims 1-12, 14-26, and 28 are pending.

Applicants are grateful for the identification of allowable subject matter in claims 13 and 27. Claim 13 and 27 have been cancelled and their limitations respectively incorporated into independent claims 7 and 21. Additionally, similar limitations have been incorporated into independent claims 1 and 16.

Each independent claim now recites a latch programming circuit which includes "a latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through..." a "latch isolation transistor." As admitted by the Office Action, the prior art is devoid of any teachings or suggestions regarding such a feature. Accordingly, independent claims 1, 7, 16, and 21 are believed to be allowable over the prior art of record. Depending claims 2-6, 8-12, 14-15, 17-20, 22-26, and 28 are also believed to be allowable for these reasons and because the combination recited in the claims are not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: March 19, 2003

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant

Version With Markings to Show Changes Made

Please amend claims 1, 7, 16, and 21 as follows:

1. A programming circuit for a plurality of programmable elements, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including

a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal;[.] and

a latch programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal, said latch programming circuit comprising,

a latch isolation transistor coupled between said programmable element and said latch circuit, and

a latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

7. A programming circuit for a programmable element, comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein said at least one latch-programming circuit further comprises, at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through one of said at least one latch isolation transistor, and

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.

16. A memory circuit, comprising:

a plurality of memory elements; and

at least one programming circuit associated with a plurality of programmable elements and

configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including

a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal;[.] and

a latch programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal, said latch programming circuit comprising,

a latch isolation transistor coupled between said programmable element and said latch circuit, and

a latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

21. A memory circuit, comprising:

a plurality of memory elements; and

at least one programming circuit associated with a plurality of programmable elements and

configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein said latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through one of said at least one latch isolation transistor;

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.